High-end Audio Playback with the Parallella

Parallella Technical Conference
Tokyo May 30th, 2015
It all started with…

• Benefits of Bi-Amping from Rod Elliott
  http://sound.westhost.com/bi-amp.htm

• Digital Room Correction from Denis Sbragion
  http://drc-fir.sourceforge.net/
Objectives

- High-Quality Audio Reproduction
- User friendly
- Low Budget
Functionalities

• “Jukebox”-like
• Digital Crossovers for a Multi-Amps setup
• Digital Room Correction
“Jukebox”-like

• Uncompressed standard CD files stored in a micro-SD card (~200 CDs in 128GB)
• Graphical User Interface to select and play the CD files
Multi-Amps setup

HiFi typical configuration

Bi-Amping configuration
Crossover Types

• Passive

• Active
  – Electronic filter
  – Digital filter (MCU or FPGA)
Digital Room Correction

Wikipedia definition

“Digital filters are applied to the input of a sound reproduction system to improve unfavorable effects of a room's acoustic”
DRC Setup

• Measure and adjust both speakers level and speakers time-alignment
• Measure the room response
• Generate the room compensation filters with Denis Sbragion’s DRC module
• Apply the correction during playback
Playback Configuration

External Hardware

- DisplayTech 320x240
- voltage divider

PL

- FPGA TFT (DMA)
- FPGA TouchPanel (FIFO)
- CPU0 NETMF User Interface WPF (managed code)
- SD drivers (DMA)

PS

- FPGA SPDIF double FIFO
- CPU1 FreeRTOS Data Processing (native code)
- SD drivers (DMA)

Parallella Micro-Server

- SanDisk Ultra 128GB microSDHC

SPDIF time base
- frequency divider 128 Fs
- SPDIF voltage translator (HP)
- SPDIF voltage translator (LP)
Playback Workflow

Cortex-A9

FPGA

DMA

64K x 2

DRC Convolution

Xover LP/HP

64K x 4

64K x 4

CDMA

BRAM0

BRAM1

SPDIF #2

SPDIF #1
Measurements Configuration

- **CPU1 FreeRTOS**
  - SD drivers (DMA)
  - SanDisk Ultra 128GB Micro-SD

- **FPGA SPDIF Out double FIFO**
  - Trigger

- **FPGA SPDIF In double FIFO**

- **SPDIF voltage translator**
  - Amplifier

- **SPDIF voltage translator**
  - Clock

- **SPDIF voltage translator**

- **Microphone ADC-SPDIF**
FPGA Programmable Logic

• LCD Interface: 8-bit parallel
• Touch Panel interface: resistive
• SPDIF in/out: simple voltage translator
• External SPDIF clock 128 Fs: high stability
• BRAM blocks: SPDIF data transfer
• Trigger to have a time-reference output to input (measurements)
Software Systems

- Graphical User Interface written in C# and running under Microsoft .NET Micro-Framework on Core #0
- Data Processing (room correction convolution and digital crossovers) written in C/C++ and running under FreeRTOS on Core #1
Microsoft .NET Micro-Framework

Advantages:

• Developing with the C# and Visual Basic .NET programming language
• A full managed execution environment with automatic memory management, multi-threading and persistent storage
• A substantial subset of the .NET Base Class Libraries including GUI classes based on the Windows Presentation Foundation
Microsoft .NET Micro-Frameowrk

Weaknesses:

• No JIT or AOT: *interpreted code is slow*
• Garbage collector can kick-in at any times: *system not deterministic*

Solution:
FreeRTOS running on Core #1 overcomes those two limitations
Parallella with SPDIF in/out
Parallella with Daughter Card
Conclusions

All Programmable SoC

Pros

• Performances
• Flexibility
• Lower Development Cost

Cons

• Complexity
• Higher Initial Cost