1st Parallella Technical Conference
Tokyo
May 30, 2015
PARALLELLA
PAST
Parallel Computing History

Ambric  Cognivue  Cswitch  SiByte  Sandbridge
Asocs  Cell  CPU Tech  Intellasys  Trips
Aspex  Coherent Logix  Cradle  IP-Flex  Rapport
Axis Semi  Clearspeed  Calxeda  Greenarrays  Silicon Hive
BOPS  ElementCXI  Icera  Inmos  Plurality
Boston Circuits  Intrinsity  Morphics  QuickSilver  Spiral Gateway
Brightscale  Octasic  PACT  Stretch  Tabula
Inmos  Mathstar  Zilabs  Xmos

Active  Chameleon

Post Mortem Interview

ZERO GENERAL PURPOSE SUCCESS STORIES!!! WHY??
IT'S THE SOFTWARE!!!

- TigerSharc DSP (1,2,3)
- Wireless Communication
- Led execution/power team
- Technology success
- Financial failure
- 100 people,$100M in losses

- ADI “ISATG” CCD interfaces
- SOC Architect/Designer
- Custom RISC architecture
- 2–3 person digital teams
- Sony, Fujifilm, Canon
- $$$,$$$ in revenue
Adapteva Before Parallella

Built World's Most Efficient Processor
$\sim$2M Total Money Spent

Epiphany0
2008
Simulation
16 cores
$0
65nm

Epiphany-I
2009
Prototype
16 cores
$200K
65nm

Epiphany-II
2010
Prototype
16 cores
$1.5M
65nm

Epiphany-III
2010
Product
16 cores
$0
65nm

Epiphany-IV
2011
Product
64 cores
$500K
28nm
But Adapteva was still dying so...
Parallella Project (Sept 2012)

- GOAL: help parallel happen
- Single Board Computer
- Credit card sized
- 2 ARM + 16/64 Epiphany cores
- 1GB RAM, GigE, uUSB, uHDMI, uSD
- ~50Gbps Total IO
- <5W
- Open source
- $99 starting price
- $898K raised
- ($3M 64core target not reached)
The Parallella Project Goal

To build a hardware platform that democratizes access to parallel computing hardware.

(affordable, open, available)
Why open?

Customers/Developers: (WIN)
- Empowers
- Reduces risk

Makers: (WIN)
- Fights FUD
- Reduces support burden
- Easier collaboration
- Enables ECO-system
- Free review / feedback
- Karma points (good will)
First Powerup
(May 2013)

- Gen0 (RevA)
- It worked!
- Power too high
- HDMI not working
- But all other design targets met!
Gen0 Shipment (July 2013)

- We build working cluster with 42 boards!
- Sent out 50 boards to early KS backers
- ~1 saw real use
- Pattern??
Chips Arrive  
(Aug 2013)
  
  - Full mask tapeout
  - New package
  - Great thermals
  - 50,000 built
  - ~90% yield!

BIG SUCCESS!!
New Investment (Dec 2013)

- Delays and cost overruns almost killed us
- $3.6M from Ericsson+VC saved the project!!
- Complete restart with new engineering team
- 5,000 waiting customers
- The worst time of my life...
Product Version (Jan 2014)

- RevC
- Supply issues stalled mass production
- Still, all shipments done by May 2014
- ~1 year late
Parallella Kickstarter Timeline

- Kickstarter Funded
- Prototypes Shipped
- Early Access Shipments
  - 100 boards shipped
  - 1,000 boards shipped
  - KS shipments completed
- General Availability
The “A1” Experiment (Jun 2014)

- International Supercomputing Conference
- 32 Parallella-64 boards
- 2,112 RISC processors
- 200 Watts
- 15 GFLOPS/Watt efficiency
- 15cm x 15cm x 68 cm
- No traction???
PARALLELLA
PRESENT
Parallella Open Source Hardware

“Microserver”
“Desktop”
“Embedded”

“Porcupine”

Ground Electronics
Parallella Open Source Software

- MPI (David Richie)
- OpenMP (University of Ioannina, Greece)
- OpenCL (David Richie)
- Erlang NIF (Mark Flemming)
- BSP (University of Utrecht, Netherlands)
- Basic (Nick Brown)
- COPRTHR / STDCL (David Richie)
- RTEMS (Hesham M. AL Matary)
- APL, Forth, Occam, Haskell (TBD, in play)
The Parallel Architectures Library

- A new “standard library” for parallel
- Compact C library with optimized routines for vector math, dsp, synchronization, and multi-processor communication.
- Designed to be portable across multiple ISAs
- Open source (apache 2.0 permissive license)
- Open invitation to participate!!
- https://github.com/parallella/pal
Parallella by the Numbers

- Over 10,000 Parallella boards shipped
- Over 6,000 boards in stock
- 200 Universities
- 17 academic publications
- 16 open source community projects
- 11 supported programming models
- 12K posts at forums.parallella.org
- Good start, but not enough
PARALLELLA
FUTURE
Parallella 2015 Plans

• Software (PAL)
  - Effort started, 5 contributors

• Fun applications
  - SDR (see demo)
  - Imaging (see Porcupine)

• Teaching
  - Programming book will be on github

• Epiphany-V
New Parallella Project Goal

To make parallel programming easy and fun!
How to Contribute?

- PAL (SW): github.com/parallella/pal
- OH (HW): github.com/parallella/oh
- Examples: github.com/parallella/parallella-examples
- Education: Teach through articles / blog posts
Let's Change Software Forever

Not a question of if, but when!
This is a once in a universe opportunity!
ANNOUNCEMENTS
Why can't we crowd source a supercomputer?

The first live test will be run at the Parallella Technical Conference in Tokyo on May 30th!
#2 New SDR Platform

- Based on RFIC AD9361
- 12 bits DACs/ADCs
- 70 MHz – 6 GHz
- RF 2 × 2 transceiver
- 56MHz BW

New Adapter Board

FCOMMS2
(from Analog Devices)
#3 New Imaging Platform

**PMOD**

**JTAG**

**Raspberry Pi Camera Interface**

48 IO

I2C

UART

elinks

WANTED!

Working Raspberry Pi Camera Module

$1000 Reward
#4 The PAL Bounty System

- A free Parallella board for every PAL function contributed
- Sponsored by Adapteva
- Math, DSP
- [github.com/parallella/pal](https://github.com/parallella/pal)

(Terms to be published at [parallella.org/pal](https://parallella.org/pal))
#5 Image Recognition Demo with supercomputer.io & Parallella

- “Naive” but educational fast convolution
- Leverages Epiphany FFT performance,
- 280 images/sec per board, still optimizing...

![Diagram](image)

13,000 IMAGES